A 3 TO 5GHZ COMMON SOURCE LOW NOISE AMPLIFIER USING 180NM CMOS TECHNOLOGY FOR WIRELESS SYSTEMS

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ABSTRACT:

A low noise amplifier plays key role in overall performance of any RF receiver. This paper presents design of low noise amplifier by using RF CMOS technology for wireless receiver systems. The proposed low noise amplifier is implemented on TSMC RF CMOS 0.18um technology. The inductive source degeneration cascaded common source topology is used in the designed low noise amplifier. The designed low noise amplifier provides minimum noise figure (NFmin) less than 0.740 dB, gain (S21) greater than 5.541 dB, input return loss (S11) less than 3dB. The designed LNA is unconditionally stable for the frequency range of 3 GHz to 5 GHz.

Keywords: Low Noise Amplifier (LNA), RF CMOS technology, common Source topology, inductive source degeneration

[1] INTRODUCTION

In future the exchange of information which directly concern with the persons will be done through wireless technology. At present there is various wireless technologies present such as mobile technology, wireless LAN, satellite communication etc. All of these technologies require radio frequency technology (RF) [1]. So in any wireless communication system the performance of RF receiver plays an important role.

A low noise amplifier plays key role in overall performance of any RF receiver as it is first building block of any RF wireless receiver as shown in [Figure-1]. Low noise amplifiers are part of receiver front end, and are used to amplify the very weak signal received by antenna [3].
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Figure 1. Typical block diagram of any wireless receiver

The main performance parameter for low noise amplifier is level of noise figure it can achieve depending on the system requirements. There are various parameters of Low Noise Amplifier that should be considered while designing such as gain, linearity, good input and output impedance matching and so on. Many fabrication technologies are available for implementing low noise amplifier such as CMOS (Complementary Metal Oxide Semiconductor), HEMT (High Electron Mobility Transistor), pHEMT (pseudomorphic Metal Oxide Semiconductor), GaN (Gallium nitride), GaAs (Gallium arsenide) etc. CMOS low noise amplifiers show more linearity as compared to GaAs and GaN technologies. As CMOS low noise amplifier operates on low power supplies there is drastic decrease in overall power dissipation of the circuit. CMOS low noise amplifiers are cost effective and use minimum chip area for fabrication.

The rest of the paper is organized as follows. In section II design methodology is discussed. Simulation results are cited in section III. Finally Conclusion is made in section IV. References are cited at last.

[2] DESIGN METHODOLOGY

2.1. Block Diagram

The [Figure-2] shows the functional block diagram of the designed low noise amplifier. Input matching and output matching Networks are the part important part of the design as it reduces the return losses which results in increased gain. Input matching is done by calculation of input impedance. Input impedance is calculated by taking the ratio of input voltage to the input current. The same concept is used for output matching. The input and output impedance matching is done at 50Ω.
2.2. Proposed LNA Design

The [Figure-3] shows the schematic of proposed LNA design. Transistors M1 and M2 form the cascode stage. The two inductors L4 and L5 forms inductive source degeneration topology shown in fig 4. This matching topology provides a perfect impedance matching without adding any noise to the system or creating any restrictions on the device gm.

2.2.1. Input Matching

Matching Networks are the very important part of any radio frequency integrated circuit. Every circuit has its own input and output impedance. The two inductors L4 and L5 are used for input matching which forms inductive source degeneration topology. The value of inductor L4 is kept low around 0.025nH. The value of inductance L5 is varied accordingly to be tuned at resonant frequency 4.29GHz. If the matching is done properly the no power is reflected back at the input side.
2.2.2. Output Matching

Output matching is responsible for the output return loss which should be very low so that LNA can achieve high gain and output power. The LC tank circuit is used for output matching. The values of passive elements is also depends upon the size of transistors which is used in the circuit for amplifying the signals.

[3] RESULTS

The designed low noise amplifier shown in [Figure-3] is simulated in Advanced Design System (ADS) tool of Agilent Systems. Note that results are totally simulation based. The simulation results are shown in [Figure-4] to [Figure-9]. There are four s-parameters that should be observed after designing the LNA. S-parameters decide the overall performance of the designed low noise amplifier. [Figure-4] shows the input return loss (S11) which gives idea about the amount of power reflected back from the source. Ideally there should be no power reflected back from the source but practically it observed to be -19.671dB at 4.175 GHz. [Figure-5] shows the output return loss (S22) which is -1.494 dB at 4.175 GHz. The designed LNA offers the gain (S21) of 10.147 dB at 4.175 GHz shown in [Figure-6]. [Figure-7] shows the isolation loss (S12) which comes out to be -26.40dB at 4.175 GHz. This graph shows that how well the input is isolated from the output.

Figure: 4. Input return Loss (S11)
The next parameter of LNA design is stability factor K. Stability factor shows whether the designed low noise amplifier is stable or not over the given frequency range. The stability factor K comes out to be greater than 1 shown in [Figure-8] therefore the designed LNA is stable over the given frequency range. Now the focus is shifted towards the most important
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parameter as far as the low amplifier concern is noise figure (NFmin). It should be as small as possible. The minimum noise figure observed to be 0.587 dB at 4.175 GHz as shown in [Figure-9].

![Figure 9. Minimum Noise Figure (NFmin)](image)

The results and specifications of designed LNA are shown in table 1.

<table>
<thead>
<tr>
<th>S.No</th>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Operating Voltage</td>
<td>0.75V</td>
</tr>
<tr>
<td>2</td>
<td>Technology</td>
<td>180 nm RF CMOS</td>
</tr>
<tr>
<td>3</td>
<td>Operating Frequency</td>
<td>4.175 GHz</td>
</tr>
<tr>
<td>4</td>
<td>S11 Input Return Loss</td>
<td>-19.671dB</td>
</tr>
<tr>
<td>5</td>
<td>S22 Output Return Loss</td>
<td>-1.494dB</td>
</tr>
<tr>
<td>6</td>
<td>S21 Gain</td>
<td>10.147dB</td>
</tr>
<tr>
<td>7</td>
<td>S12 Isolation Loss</td>
<td>-26.40dB</td>
</tr>
<tr>
<td>8</td>
<td>Minimum Noise Figure</td>
<td>0.587dB</td>
</tr>
</tbody>
</table>

Table: 1. CMOS Low Noise Amplifier Specifications

[4] CONCLUSION

Implementing low noise amplifier in CMOS technology is considered a major step towards the realization of a complete receiver on chip. In this paper a low noise amplifier circuit has been designed and simulated for the frequency range of 3 GHz to 5 GHz by using Advanced Design System (ADS) 2009 software. The proposed LNA has forward gain greater than 5.5 dB and minimum noise figure less than 0.740 dB.

REFERENCES


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