POWER OPTIMIZATION AT NANOSCALE USING FINFETS AND ITS COMPARISON WITH CMOS

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ABSTRACT:

Amount of power consumption is one of the important measures of performance of an integrated circuit. CMOS is the latest technology which is in use till date. This paper gives an overview of the power dissipation occurring in CMOS circuit. The paper then describes the advantages and limitations of power optimization techniques of CMOS. As we go deeper into the nanometer scale, MOS transistors face many limitations such as Short Channel Effects (SCEs), Drain Induced Barrier Lowering (DIBL) and subthreshold leakage. Multigated MOS devices prove to be a better solution to these problems. Thus FinFET device along with various power optimization techniques using FinFETs is described. At the end a comparison of the simulation results at 45nm based on the factors of leakage current, leakage power and delay is given. These results show that FinFET gives better power optimization than MOS transistor at nanoscale.

Keywords: FinFETs, Leakage power, Power optimization, Low power nanoscale design, Scaling limitations, Back gate biasing, Dual V_T, Asymmetric Φ_G

[1] INTRODUCTION

First MOS microprocessor was created in 1970. Since then the technology went on advancing at a great pace. According to the Moore's law, the number of transistors in a unit chip area double every two years. This is enabled by the miniaturization of the transistor device. But this miniaturization has to face and overcome many issues at every stage of its progress. The earliest microprocessor, created in 1970, was entirely made of MOS transistors. It was fabricated at 10um technology node. In 2008 the semiconductor manufacturing process had reached 45nm technology node. And now, in 2014, the aim is to reach 14nm technology node. But this progress is obstructed by many unwanted effects which emerge in MOS devices in the nanometer regime. The scaling down of MOS transistor has many limitations as increase in leakage current, increase in power dissipation, V_T roll-off, interconnect capacitance, short channel effects and DIBL.
The need for devices that consume a minimum amount of power was a major driving force behind the development of Multi-Gate transistor technologies. This paper aims to explore FinFET and its characteristics of power reduction.

The second section addresses the power dissipation phenomenon in CMOS. Types of power dissipation, leakage current mechanisms, ways of power optimization and limitations of MOS scaling are discussed in this section. The paper then describes the FinFET technology in brief. Here the discussion will be focused on the advantages of using FinFET for low power applications as compared to MOS transistor.

The forth section explains the simulation setup. An Inverter circuit is modeled using both MOS devices and FinFET devices in LTspiceIV tool from Linear Technology. This circuit is implemented at 45nm technology node. These circuits are then analyzed and compared on the basis of leakage current, leakage power and delay.

[2] POWER CONSUMPTION IN CMOS GATES

Managing the power utilization of a circuit is an issue that must be handled at all levels of abstraction starting from the circuit level to the system level. The different low power CMOS design techniques are discussed here. For this purpose, the power consumption of a basic CMOS circuit is described first and then a review of the low power design techniques is given.

[2.1] POWER DISSIPATION PHENOMENON

The power dissipated in a CMOS circuit can be categorized to be either static power or dynamic power. Ideally, during operation, the pull-up and pull-down circuitry is never on simultaneously. Hence the static power is only contributed by the leakage current.

\[ P_{\text{stat}} = I_{\text{leakage}} \times V_{\text{DD}} \]

where \( I_{\text{leakage}} \) is the total leakage current flowing through the circuit and \( V_{\text{DD}} \) is the supply voltage.

Most of the power consumption occurs during switching. This is the dynamic power dissipation and can be given by,

\[ P_{\text{dyn}} = C_{L} \times V_{\text{DD}}^2 \times f \]

where \( C_{L} \) is the load capacitance and \( f \) is the switching frequency.

[2.2] LOW POWER CMOS DESIGN TECHNIQUES AND THEIR LIMITATIONS

Rabaey [1] has described the low power design techniques of CMOS by reducing the supply voltage, reducing the threshold voltage, reducing the effective capacitance and reducing the power of clocking system. Reducing the supply voltage increases the delay. Delay increases by seven times when \( V_{\text{DD}} \) is decreased from 5 volts to 1 volt. The threshold
voltage cannot be reduced below a certain value to avoid subthreshold leakage current. Other methods require additional circuitry to be added which affects the area of the circuit.

[2.3] CMOS LIMITATIONS TO SCALING

CMOS circuits give good results at few hundreds of nanometers technology nodes. But further scaling down of MOS transistor imposes many limitations.

The short channel effects (SCEs) occur mainly due to the limitation imposed to the drift of electrons in the channel. Drain Induced Barrier Lowering (DIBL) takes place when a high voltage is applied to the drain. At such times, source injects carriers into the channel region irrespective of the gate voltage.

Another effect called hot carrier injection occurs in short channel devices. Due to a high electric field at the oxide interface, electrons in the gate can acquire enough energy and inject into the oxide layer giving rise to gate leakage current.

Punchthrough is another effect occurring as a result of short length of the channel. Increased reverse bias across the junctions further decreases the separation and the depletion regions merge so that the majority carriers in the source reach the drain and punchthrough takes place. Moreover other effects such as Band to Band Tunneling (BTBT), Gate Induced Drain Leakage (GIDL) and gate oxide tunneling occur in MOS transistor due to scaling.

[3] FINFET

A planar FinFET is shown in [Figure-1]. A FinFET is a FET in which the channel is turned on its edge and made to stand up. The two gates of a FinFET can be made independently controllable by etching away its top part. Such a FinFET is called an independent-gate (IG) FinFET, whereas when the two gates of the FinFET are shorted, the FinFET is called a shorted-gate (SG) FinFET, or sometimes tied-gate FinFET [2].

![Figure: 1. A FinFET [2]](image)

SG FinFETs provide improved drive strength and control of the channel. Thus, logic gates based on SG FinFETs are the fastest. On the other hand, the voltage bias in an IG
FinFET can be used to linearly modulate the threshold voltage of the front gate. This phenomenon can be used to reduce the leakage power of the logic gate based on IG FinFETs by one to two orders of magnitude by reverse-biasing their back gates. This, however, comes at the price of increased logic gate delay.

[3.1] FINFET AS A SOLUTION FOR LOW POWER DESIGN

Three design techniques namely, back-gate biasing, dual-$V_T$ and asymmetric-$\Phi_G$ are reviewed in this section.

[3.1.1] BACK-GATE BIASING

Swahn and Hassoun describe in [3] that back-gate biasing of a FinFET is as effective as Adaptive Body Biasing (ABB) in CMOS. ABB is an effective technique to reduce $V_T$ variability, reducing leakage current and thus energy. By applying different voltages to the two gates of a FinFET both the threshold voltage and the leakage current can be changed. Thus an effect similar to ABB can be achieved.

Agostinelli et al [4] have studied the advantages offered by multi-gate FinFETs over traditional bulk MOSFETs when low standby power circuit techniques are implemented. They simulated various circuits, ranging from ring oscillators to mirror full adders, to investigate the effectiveness of back biasing in both FinFETs and bulk MOSFETs. The dependence of $V_T$ on back-gate biasing is analyzed for both MOSFETs and FinFETs. It has been proved that the dependence of $V_T$ is three times larger in FinFETs and also the sensitivity of $V_T$ to back-biasing is decreasing in MOS technology at each process generation.

[3.1.2] DUAL-$V_T$

Rostami and Mohanram [5] have proposed the design of dual-$V_T$ independent gate FinFETs by optimizing the oxide thickness, electrode work-function, silicon thickness, and gate-source/drain underlap. It is shown that the dual-$V_T$ independent-gate FinFETs enable merging of series and parallel transistors, with efficient realization of logic gates. Results on several benchmark circuits demonstrate that significant savings in total power consumption can be achieved by incorporating these gates into the technology library.

[3.1.3] ASYMMETRIC-$\Phi_G$

Bhoj and Jha [6] have introduced Asymmetric-$\Phi_G$ FinFETs and demonstrated that they possess steep subthreshold characteristics. Thus they can provide low leakage current at the same time give high speed performance and hence they can be employed in the design of ultra-low-leakage logic circuits in high performance process technologies.

[Table-1] summarizes the advantages of these design techniques.

<table>
<thead>
<tr>
<th>Design Technique</th>
<th>Effectiveness in Power Optimization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Back-Gate Biasing</td>
<td>Reduces $V_T$ variability</td>
</tr>
<tr>
<td></td>
<td>Reduces leakage and</td>
</tr>
<tr>
<td></td>
<td>Reduces power</td>
</tr>
</tbody>
</table>
Dual-$V_T$ Enables merging of series and parallel transistors and Saves total power consumption.

Asymmetric-$\Phi_G$ Low leakage current and High speed performance

<table>
<thead>
<tr>
<th><strong>Parameter</strong></th>
<th><strong>Value</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel length</td>
<td>45nm</td>
</tr>
<tr>
<td>Oxide Thickness</td>
<td>1.5nm</td>
</tr>
<tr>
<td>Si thickness</td>
<td>8.4nm</td>
</tr>
<tr>
<td>Threshold voltage of front gate</td>
<td>0.31V</td>
</tr>
<tr>
<td>Threshold voltage of back gate</td>
<td>0.31V</td>
</tr>
<tr>
<td>Channel doping</td>
<td>$2\times10^{16}$ cm$^{-3}$</td>
</tr>
</tbody>
</table>

Table: 1. Review of FinFET Design Techniques

[4] SIMULATION AND DISCUSSION

LTspiceIV software is used to design and to obtain the characteristic for 45nm FinFET based on the specifications. An in-built model for the FinFET device is not available in the library of this spice software. Therefore, the PTM model developed by [7] has been used in order to prove the claims of power minimization in FinFET.

An inverter circuit is implemented using the FinFET model and CMOS model designed using above mentioned parameters.

[Figure-2] shows the leakage current in the front gate of FinFET NMOS at 45nm node. It reveals that the current is exponentially dependent on the gate voltage and it reaches the maximum of $0.0012fA$. 

Table: 2. Parameter specification for FinFET model at 45nm node
Figure: 2. Leakage current in the front gate of FinFET NMOS at 45nm node

[Figure-3] shows the comparison of leakage currents in both the circuits. It proves that the leakage current is reduced from 600nm in CMOS inverter to 0.0012fA in FinFET based inverter.

Figure: 3. Leakage currents in the gate of NMOS in a FinFET and a CMOS inverter at 45nm node

[Figure-4] compares their voltage transfer characteristics. It is evident from this comparison that CMOS inverter has a more ideal VTC than the FinFET based inverter.
[5] CONCLUSION

The low power design techniques for FinFET implementing back-gate biasing, dual-$V_T$ and asymmetric-$\Phi_G$ are reviewed. It has been observed that these techniques provide better power optimization by reducing leakage current, by reducing $V_T$ variability and by optimizing circuit area. It has been proved with the help of simulation results that FinFET based inverter provides reduction in leakage current. Thus leakage power is reduced and power optimization is achieved. However, the voltage transfer characteristics of FinFET is slower than that of CMOS and thus FinFET circuit results in larger delay as compared to CMOS.
REFERENCES


Authors’ brief introduction -

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