A LOW POWER NON-VOLATILE LUT BASED ON FRAM
Pavani kodamanchili1, Prema Kumar Medapati2

1,2Department of Electronics and Communications,
Shri Vishnu Engineering College for Women, Autonomous Bhimavaram, INDIA

ABSTRACT:
The Emerging non-volatile memories such as MRAM (Magnetic Random Access Memory) PRAM, and RRAM have been widely investigated to replace SRAM as the configuration bits in FPGA but this brings reliability issues in order to overcome this RRAM slice is introduced but it consumes more power hence the FRAM cell is proposed in order to reduce the power.

Keywords: Logic in memory, low power, NVLUT, FRAM (Ferro electronic Memory)

[1] INTRODUCTION

During the last decades SRAM (Static Random Access Memory) has been widely used but the volatility of SRAM has limited FPGAs (Field Programmable Gate Arrays) in applications, where high security and long redemption and immediate power on are required. The problem is being solved by using the non-volatile memories. The non-volatile memories such as MRAM (Magnetic Random Access Memory), PRAM (Programmable Random Access Memory) and RRAM (Resistive Random Access Memory) have been justified with improved scalability and logic compatibility, and when considering the logic in memory concept look up table has been designed with the NVMs (Non Volatile Memory) which is the core building block of the FPGA. Different non-volatile SRAM structures with MRAM and RRAM have been considered to straightly reinstate SRAM in the LUT to gain non volatility but the size of the nvSRAM cell is
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significantly greater than that of SRAM, and write disorderness is also crucial to abstain for half selected RRAM cells.

And next when coming to the RRAM, SAKOMOTO [1] suggested a NVLUT based on the Nano Bridge, coming to the operation the programming path of the Nano Bridge stakes the same multiplexer with the logic path by accomplishing the size of the transistors in the multiplexer, they are appreciable greater than in order to mollify the reset voltage for Ron

By considering MRAM, SUZUKI [2] proposed a two-input NVLUT based on MRAM in the current mode logic for low power. ZHAO [3] proposed another type of MRAM based NVLUT for run-time reconfigurations.

REN [4] suggested a third type of NVLUT based MRAM which was named as hybrid LUT2. But in this type the Roff/Ron of the MRAM is lesser in compared to the PRAM and RRAM, whose output gives the smaller sense margin or more area, because of the serial and parallel magnetic junctions. Furthermore the first three types of MRAM based NVLUT has a mismatch in the parasitic RC, in between the preferred line in the multiplexer and the reference path, which may cause the NVLUT to fail. Next coming to the hybrid LUT2 the configuration of MRAM cells claims the same decoding circuit with the logic operation, whose inputs may be equipped to the other logic blocks, and cannot be recycled as the address inputs during configurations.

Next in [5] suzuki proposed a six input NVLUT by using the serial/parallel magnetic junctions in order to get sufficient sensing margin.

CHEN [6] suggested another type of RRAM based NVLUT by making the usage of the crossbar array, but sneaking currents in the crossbar array brings greater leakage and very low sensing margin. By considering the above survey none of them has achieved the reliability against the memory and logic variations, low power and low leakage at the same time.

Xiaoyong[7] Proposed the low power nvLUT based on the RRAM slice which consists of 1T1R(one transistor one resistor),SSAVC(Single Stage Sense Amplifier),MRP(Matched Reference Path),TMUX(Tree Multiplexer) and a Footer transistor, by making use of these blocks the nvLUT was designed and the reliability is achieved but consumes more this can be overcomed.

[2] EXISTING METHOD OF NVLUT BASED ON RRAM
The existing nvlut consists of a SSAVC (Single Stage Sense Amplifier Voltage Clamp) which converts the resistance state of RRAM (Resistive Random Access Memory) into rail-to-rail logic voltage. The transistors M3-M6 constitute a latch Amplifier. Transistors M1 and M2 are used to precharge the output nodes. The internal voltages in the TMUX and MRP are clamped to lower voltages by the clamp transistors to save power trimming the Rref can help to disabuse the parasitic resistance mismatch between the selected path in the TMUX and the reference path, their parasitic capacitance cannot be easily estimated and compensated. The MRP device is used to minimize the parasitic mismatch. The header transistor is used to select the corresponding RRAM. The 1T1R (one Transistor one resistance) RRAM cell is employed as the configuration bit and a reference resistor to provide sufficient sense margin. The 1T1R RRAM cell can eliminate the sneaking current and the disturbances during the write and the read, thus saving the power and acquiring the high yield. The Footer Transistor is used to initiate the conversion of the clock. nvlUT based on RRAM slice the power is reduced to only some extent the power can be reduced better than the RRAM by using the FRAM.

[3] PROPOSED METHOD OF NVLUT BASED ON FRAM

In order to rectify the problems mentioned above the NVLUT in the existing method it consists of RRAM slice it is replaced by FRAM in the proposed method. Instead of using the footer transistor the header transistor is used. It consists of a Header Transistor, SSAVC (Single Stage Sense Amplifier), TMUX (Tree Multiplexer), MRP (Matched Reference Path), FRAM (Ferro Electronic Random Access Memory) slice.
3.1 Header Transistor

The header Transistor is implemented by PMOS transistors to control Vdd supply. PMOS transistor is less leaky than NMOS transistor of a same size. In order to reduce the power instead of the footer Transistor the Header Transistor is used.

3.2 Single Stage Sense Amplifier Voltage Clamp (SSAVC)

The Single Stage Sense Amplifier is the second block of the nVlut. It has a low power dissipation and a sense of basic Differential amplifier in comparison to the offset voltage. The simultaneous exchange of equipment, providing fast load-sensing operation, the Sense voltage Differential is the primary purpose of the amplifier. SSAVC converts the FRAM state.
3.3 Tree Multiplexer (TMUX)

The Tree Multiplexer is the third block of the nvlut FRAM. It consists of the two inputs IN0, IN1, those two inputs are used to select the FRAM. The TMUX is one of the LUT which performs the NOR operation.
3.4 Matched Reference Path (MRP)

The parasitic resistance mismatch between the paths in the TMUX cannot be easily estimated and compensated. The MRP is devised to minimize the parasitic RC mismatch. The two reference paths are P01 and P ref, for reliable sensing the parasitic RC’s of P01 and P ref should be equivalent and hence the transistors in the MRP take the same size, to imitate the parasitic effects of the OFF state transistor in the Tree Multiplexer.

![Figure 5. Structure of MRP](image)

3.5 FRAM Slice (Ferroelectric Random Access Memory)

FRAM is a Non-Volatile Memory, A Ferroelectric memory cell consists of a ferroelectric capacitor and a MOS transistor it is similar to the DRAM (Dynamic RAM) FRAM memory cell also known as 1C1T (one capacitor one transistor) FRAM allows systems to retain information even when power is lost without restoring to batteries, EEPROM, or Flash, It is less expensive than Magnetic memories, it is a memory of 4MB The FRAM offers a unique set of features related to other memory technology.

![Figure 6. Schematic of FRAM slice](image)

[4] SCHEMATIC OF THE NVLUT BASED ON FRAM USING CADENCE

The Overall architecture of the nvlut based on FRAM was implemented using the cadence virtuoso tool in 180nm technology the components of the transistors are taken from the gpdk180 and the capacitors and the input pulses are taken from the analog library. The Overall circuit is constructed and checked the schematic check was correct. The figure below shows the schematic of the NVLUT based on FRAM.
4.1 Output Waveforms of the nvlut based on FRAM

Figure 7. Schematic of NVLUT based on FRAM

Figure 8. Output Waveforms of NVLUT based on FRAM when clk=1 out=0 outb=1
4.1 layout of the nvlut FRAM slice

![Diagram of nvlut FRAM slice]

Figure 9. Overall Layout of nvLUT based on FRAM

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Power</th>
<th>Layout Area(µm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NVLUT based on RRAM (Existing method)</td>
<td>1.007mW</td>
<td>367.82</td>
</tr>
<tr>
<td>NVLUT based on FRAM (Proposed method)</td>
<td>428.8µW</td>
<td>531.824</td>
</tr>
</tbody>
</table>

Table 1: Comparision of existing and proposed method

[5] CONCLUSION

The NVLUT based on the FRAM was designed in order to reduce the power which performs better than RRAM slice, FRAM allows systems to retain information even when power is lost without restoring to batteries it is faster, than the other memories and it is the fastest memory with very low power requirement, and the MRP which reduces the parasitic RC mismatch.
REFERENCES


